AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at line 4 on page 4 with the following amended paragraph:

FIG. 2 is a diagram of a SRAM device according to an example arrangement. Other arrangements and configurations are also possible. More specifically, the SRAM device 100 includes a memory array (M rows and N columns) 140 of memory cells. The SRAM device 100 may also include a row decoder 115, a timer device 120 and I/O devices (or I/O outputs) 130. Bits of the same memory word may be separated from each other for efficient IO design. In this example arrangement, each of the N columns corresponds with 8 bit lines (or 8 bit-pairs). For example, each column includes bit lines b0 b1, b2, b3, b4, b5, b6 and b7. Each of the bit lines includes a bit line pair. For example, bit line b0 includes bit line pair b10 and b10#. Also, bit line b7 includes bit line pairs b17 and b17#. The other bit line pairs are not labeled in FIG. 2 for ease of illustration. A plurality of sense-amplifiers $SA_{0\text{-}n}$ (n=(N/8)-1) may also be provided such that each group of eight columns may share a single sense amplifier SA. An 8-to-1 multiplexer (MUX) (not shown) may be used to connect each column to the SA during a READ operation. Another 8-to-1 MUX (not shown) may be used to connect each column to a write driver during a WRITE operation.